^{60}Co γ-ray irradiation experiments and electrical modeling of TSVs in 3D ICs*

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Three-dimensional (3D) integration using through-silicon vias (TSVs) has emerged as a key technology for extending Moore's Law as transistor scaling approaches physical limits. However, ensuring the electrical reliability of TSVs in radiation environments remains a critical challenge. This study investigates the impact of total ionizing dose (TID) irradiation on the transmission performance and parasitic effects of the TSV channel. Three types of test samples with varying sizes and TSV arrangements were fabricated and subjected to ^{60}Co γ-ray irradiation. S-parameters were measured across different doses. Experimental results indicate that increasing irradiation dose leads to greater insertion loss, a narrower -1 dB bandwidth, a higher rate of change of group delay, longer propagation delay, and a reduced peak to peak of group delay. At 180 krad(Si), the maximum increase in propagation delay is 1.58%, the maximum average rise in the rate of change of group delay is 2.52%, and the maximum reduction in peak to peak of group delay is 32.48% compared to pre-irradiation. In addition, TID compresses the frequency response of S_{21} magnitude, shifting dominant effects to lower frequencies. To quantify the impact of TID on the electrical parameters and material properties of TSVs, an equivalent circuit topology considering crosstalk effects was first developed. Optimization was then performed in an Advanced Design System (ADS) using the validated equivalent circuit to extract changes in parasitic parameters. The optimization results indicate that increasing irradiation dose leads to higher silicon substrate capacitance, crosstalk capacitance, and oxide layer capacitance, while silicon substrate conductance and crosstalk conductance decrease. These changes are attributed to TID-induced modifications in the material properties of the TSV channel. Subsequently, polynomial fitting was employed to establish functional relationships between material properties and irradiation dose. As a result, a dose-dependent electrical model for TSVs was developed. This work provides a guiding strategy for evaluating the electrical behavior of TSVs under irradiation and contributes to the design of irradiation tolerant 3D integrated circuits (ICs) for high reliability applications.

Keywords: Total ionizing dose, Through silicon via, S-parameters, Equivalent circuit model, Electrical parameters

I. INTRODUCTION

As Moore's Law approaches its physical constraints in transistor scaling and wafer manufacturing [1], the demand for high-performance chips continues to rise, fueled by advancements in information technology and emerging industries. In aerospace applications, these chips face challenges such as limited interconnect bandwidth (BW), integration density, and power efficiency [2–4]. To address these post-Moore's Law demands, three-dimensional (3D) integration technologies including active integrated circuit (IC) 3D integration, 2.5D integration with passive interposers, and heterogeneous chip integration have emerged [5, 6]. Among these, through silicon via (TSV) technology, a vertical interconnection method, is pivotal. TSVs provide key benefits, including shorter interconnects, reduced power consumption, and higher package density, enabling device miniaturization and multifunctionality [7–9]. Recent innovations, such as novel materials and fault-tolerant designs, further enhance TSV performance [10–12].

Despite these advancements, ensuring TSV reliability in radiation environments remains a critical challenge. Key limitations include noise coupling between aggressive/victim TSVs [13], thermal management inefficiencies in stacked layers [14–16], and material-induced stress mismatches [17]. Understanding the impact of total ionizing dose (TID) on TSV behavior is essential for advancing 3D ICs. This is particularly critical in aerospace applications, where radiation tolerant designs are required [18–21]. A TSV comprises a vertical metal interconnect (typically copper) passing through a silicon substrate, surrounded by an insulating dielectric layer (commonly SiO_2) to prevent copper ion diffusion into silicon. This configuration forms a metal-oxide-semiconductor (MOS) structure, which is highly sensitive to ionizing radiation, necessitating rigorous evaluation for aerospace applications [22–31].

Multiple studies on the TID effect in MOS structures shown that γ-ray irradiation induces charge trapping and accumulation in the oxide layer, resulting in leakage currents [32–35]. These leakage currents, along with MOS capacitance changes, contribute to signal delays and power losses in TSVs. Zeng et al. demonstrated that positive charges trapped in the oxide layer increase leakage currents and reduce the coupling capacitance in TSV arrays [38, 39]. Tian et al. examined the affects of high-energy heavy ion irradiation on TSVs, simulating the electrical performance of silicon dielectric layers subjected to varying ion energies [40]. Li et al. predicted that TSV processes alter the charge trapping behav-

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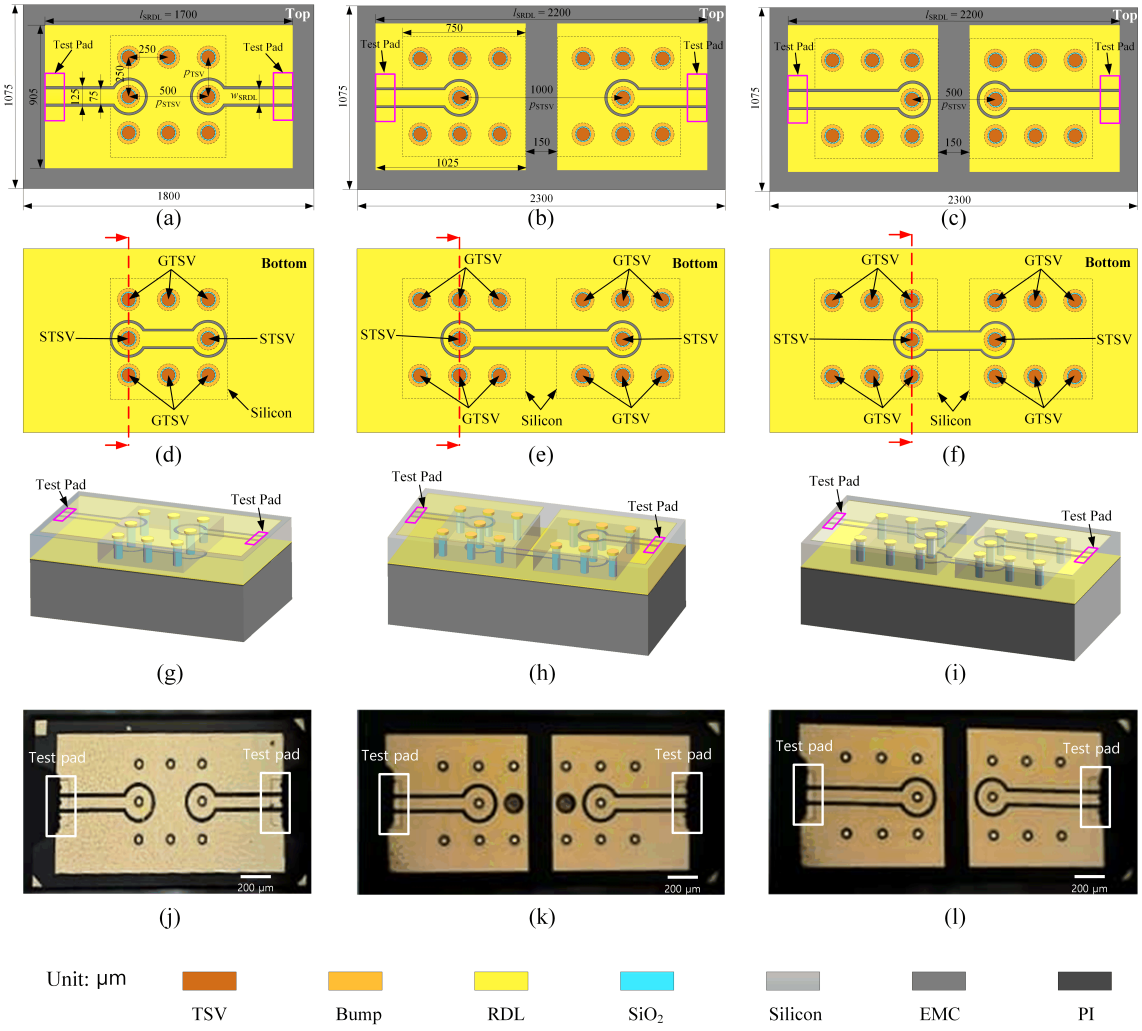


Fig. 1. (a) Top-view of sample A, (b) top-view of sample B, (c) top-view of sample C, (d) bottom-view of sample A, (e) bottom-view of sample B, (f) bottom-view of sample C, (g) 3D view of sample A, (h) 3D view of sample B, (i) 3D view of sample C, (j) photograph of sample A, (k) photograph of sample B, and (l) photograph of sample C. These 3D views show the signal pathways of the TSV sample. The bottom EMC is used to support the sample. The objects are not drawn to scale.

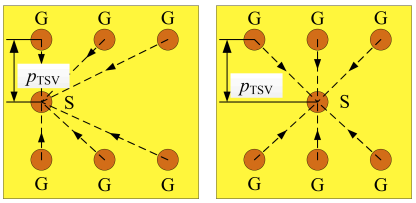


Fig. 2. Distribution of STSV with surrounding GTSVs: (a) Sample A and C and (b) Sample B. These distributions are used to calculate $p_{\mathrm{TSV\_Total}}$.

ior in the gate oxide layer, though experimental results indicated minimal impact [41]. Combined experimental and simulation approaches revealed a dose-dependent leftward shift in capacitance-voltage (C-V) curves shift leftward after irradiation [42, 43], correlating with degraded TSV performance, notably a decline in the S_{21} parameter. Yang et al. developed a one-dimensional (1D) model using finite element analysis in COMSOL Multiphysics to further explore TID effects on TSVs [44]. Their simulations, validated by component design and irradiation experiments, revealed nonlinear TID effects on TSV devices. Specifically, the S_{21} parameter worsened with increasing irradiation dose, although the magnitude of S_{21} ($|S_{21}|$) variation diminished at higher doses.

Focusing on the dielectric loss of SiO_2/Si heterostructures, Ref. [45] investigates the impact of TID irradiation on the alternating current (AC) characteristics of TSVs. The study found that irradiation induced a dielectric loss peak in TSVs, which shifted to lower frequencies with increasing irradiation doses. Using the Maxwell-Wagner interfacial relaxation model, the study attributes this loss to the formation of boundary oxide traps (BTs). Similarly, Ref. [46] reported that ^{60}Co γ-ray irradiation on dual-channel and array TSV test chips

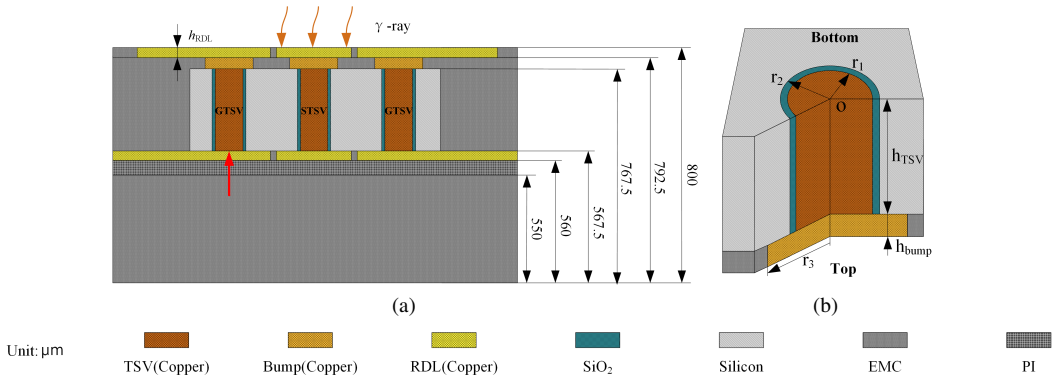


Fig. 3. (a) Cross-section view along the red dashed line of Figs. 1(d)–(f) and (b) Bottom view of a single TSV in Fig. 2(a). The objects are not drawn to scale.

Table 1. Design parameters of TSV samples.

Samples	Fixed parameters (μm)							Variable parameters (μm)			
	r_1	r_2	r_3	h_{TSV}	h_{Bump}	w_{SRDL}	h_{RDL}	p_{STSV}	$p_{\mathrm{TSV\_Total}}$	l_{SRDL}	FMSS
A								500	$2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$	1700	Silicon
B	35	35.5	50	200	25	75	7.5	1000	$2(1+2\sqrt{2})p_{\mathrm{TSV}}$	2200	Silicon and EMC
C								500	$2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$	2200	Silicon and EMC

led to a reduction in parasitic MOS capacitance and signal transmission efficiency at higher doses. The analysis revealed that TID-induced oxide and interface state trap charges lower the flat-band voltage, resulting in impedance discontinuities and signal integrity (SI) issues. Recent advancements in TSV fault tolerance, including broadcast-TDMA mechanisms [17] and honeycomb-based redundancy designs [11, 47], demonstrate promising approaches to mitigate reliability challenges, though their applicability in radiation-hardened environments remains unexplored.

Existing studies on TID effects in TSVs have primarily focused on direct current (DC) leakage, I-V and C-V characteristics, AC behavior, and scattering parameters (S-parameters). While these studies provide valuable insights, critical aspects such as the relationship between frequency response, propagation delay, and design parameters under TID remain underexplored. Furthermore, the interplay between parasitic electrical parameters and material properties under TID has not been fully investigated, particularly in high-frequency regimes where noise coupling effects become pronounced [12, 13]. Recent work on THz-frequency TSV interference minimization using benzocyclobutene (BCB) liners highlights the need for frequency-aware radiation hardening strategies [48].

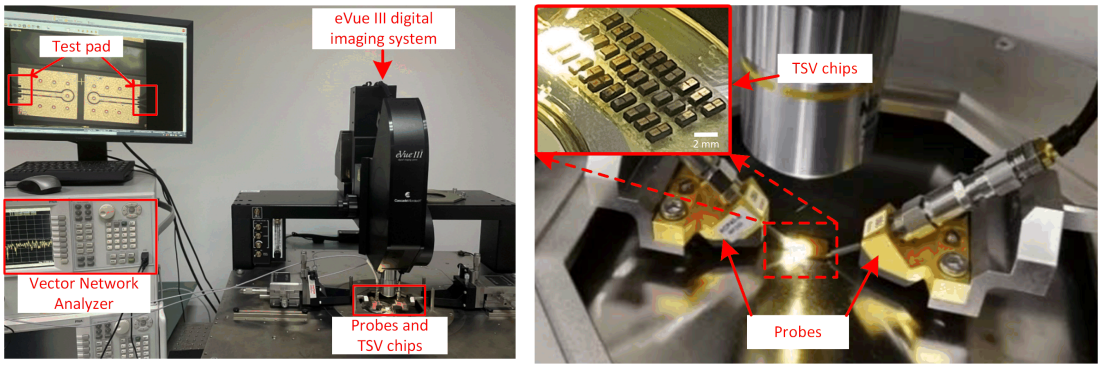
To address these gaps, this paper develops a predictive S-parameter model that relates TSV design parameters to TID-induced material property changes. This model is then applied to quantify the effects of TID on the parasitic electrical parameters and material properties of TSV channels. The paper is organized as follows: Sect. II outlines the design of three TSV sample types, including bumps and redistribution layers (RDLs), and the setup of the ^{60}Co γ-ray experiments. Sect. III analyses the S-parameters, -1 dB BWs, design-dependent frequency responses, group delay, and propagation delay based on experimental data. Sect. IV introduces an equivalent circuit model for the TSV channel, extracts TID-dependent parasitic parameters, and quantifies TID effects on material properties, enabling an S-parameter prediction model linked to design and material variations. Sect. V explores future directions by assessing the limitations of the proposed model, comparing this work with previous studies to highlight its novelty, and proposing refinements for future research. The paper concludes in Sect. VI.

II. TSV SAMPLE DESIGN AND EXPERIMENTS SETUP

Heterogeneous integration in 3D ICs combines vertical interconnections (bumps) with horizontal routing (RDLs). A comprehensive analysis of TSVs must therefore consider both the TSVs and their interactions with these components, as they are critical for signal transmission and overall system performance.

A. TSV Sample Design

Three types of TSV samples with varying bump and RDL sizes and layouts were designed. Top and bottom views of the samples are shown in Figs. 1(a) – (f). Sample A measures 1800 $\times$ 1075 μm and includes six ground TSVs (GTSVs), while Samples B and C share identical dimensions (2300 $\times$ 1075 μm) and include twelve GTSVs each. Their 3D views are illustrated in Figs. 1(g) – (i). Photographs of the chips are shown in Figs. 1(j) – (l).



(a) (b)

Fig. 4. (a) Testing environment of the TSV chips [44] and (b) Probes and TSV chips.

The TSV fabrication process consists of several key steps, including the formation of TSV vias using deep reactive ion etching (DRIE), the deposition of a SiO_2 insulating layer on the via sidewalls, and the electroplating of copper to fill the vias. This is followed by moulding, the formation of a backside RDL, wafer thinning and the formation of a frontside RDL.

Measuring TSV S-parameters on a bare wafer is challenging due to the TSV ports being located at opposite ends of the wafer. To address this, ground RDLs (GRDLs) connect the top and bottom ports of all GTSVs to ensure consistent grounding across the array. Similarly, signal RDLs (SRDLs) link the bottom ports of signal TSVs (STSVs), enabling signal transmission between two STSVs through their respective bumps.

Although all three types of TSV samples feature the same number of GTSVs surrounding a single STSV, their arrangements differ. The shielding effect provided by the GTSVs is influenced by the pitch between the GTSV and the STSV [49–53]. This total pitch, denoted as $p_{\mathrm{TSV\_Total}}$, quantifies the shielding effect. According to the schematic in Fig. 2, $p_{\mathrm{TSV\_Total}}$ is calculated as $2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$ for samples A and C, and $2(1+2\sqrt{2})p_{\mathrm{TSV}}$ for sample B.

The cross-section along the red dashed lines in Figs. 1(d) – (f) is shown in Fig. 3(a), while Fig. 3(b) illustrates the bottom view of a single TSV embedded in a silicon substrate. In this diagram, r_1 represents the TSV radius, r_2 the oxide layer radius, r_3 the bump radius, h_{TSV} the TSV height, and h_{bump} the bump height. These parameters were predefined as fixed design elements in this study. Variable parameters were also introduced to enable controlled analyses and to explain variations in the experimental results.

As shown in Fig. 1, samples A and C share the same STSV pitch (p_{STSV}) but differ in their SRDL lengths (l_{SRDL}). Conversely, samples B and C have the same SRDL length but differ in p_{STSV}. Consequently, $p_{\mathrm{TSV\_Total}}$, p_{STSV}, and l_{SRDL} were defined as variable parameters. In addition, in sample A, the two STSVs are located on the same silicon substrate, where the filling material between the STSVs (FMSS) is silicon. In contrast, in samples B and C, the STSVs are on separate silicon substrates, with an epoxy molding compound (EMC) layer providing isolation. A summary of the design parameters is presented in Table 1.

Table 2. Experimental conditions of TID irradiation.

Conditions	Value
Radiation sources	^{60}Co
Dose rate	50 rad(Si)/s
Dose point	60 krad(Si), 120 krad(Si), 180 krad(Si)
Temperature	25°C
Measurement equipment	Microwave probe stations and vector network analyzer

B. TID Experiments Setup

Irradiation experiments were performed using a ^{60}Co γ-ray source at the Northwest Institute of Nuclear Technology, with a dose rate of 50 rad(Si)/s. Dose levels were set at 60, 120, and 180 krad(Si). All TSV samples were irradiated without any applied bias. A total of 27 samples were prepared, with nine allocated to each of the three TSV types (labeled A1# – A9#, B1# – B9#, and C1# – C9#). For each TSV type, three samples were irradiated at each dose level. A summary of the experimental conditions is presented in Table 2.

Signal transmission begins at the test pad located on one side of the top SRDL and propagates to the upper surface of the first STSV. From there, it travels through the TSV to its lower surface and is transferred via the bottom SRDL to the lower surface of the second STSV. The signal then passes through the second TSV to its upper surface and continues along the top SRDL to the measurement pad on the opposite side. The upper surfaces of the two STSVs are connected to the sample edges via two top SRDLs, forming a ground-signal-ground (GSG) test pad alongside adjacent GRDLs, as shown in Figs. 1(a) – (c), (g) – (i). The SRDLs and GRDLs are separated by an EMC layer on the same plane.

The testing environment is shown in Fig. 4(a). Custom-designed GSG probes were used to minimize errors associated with conventional soldering and simplify measurements.

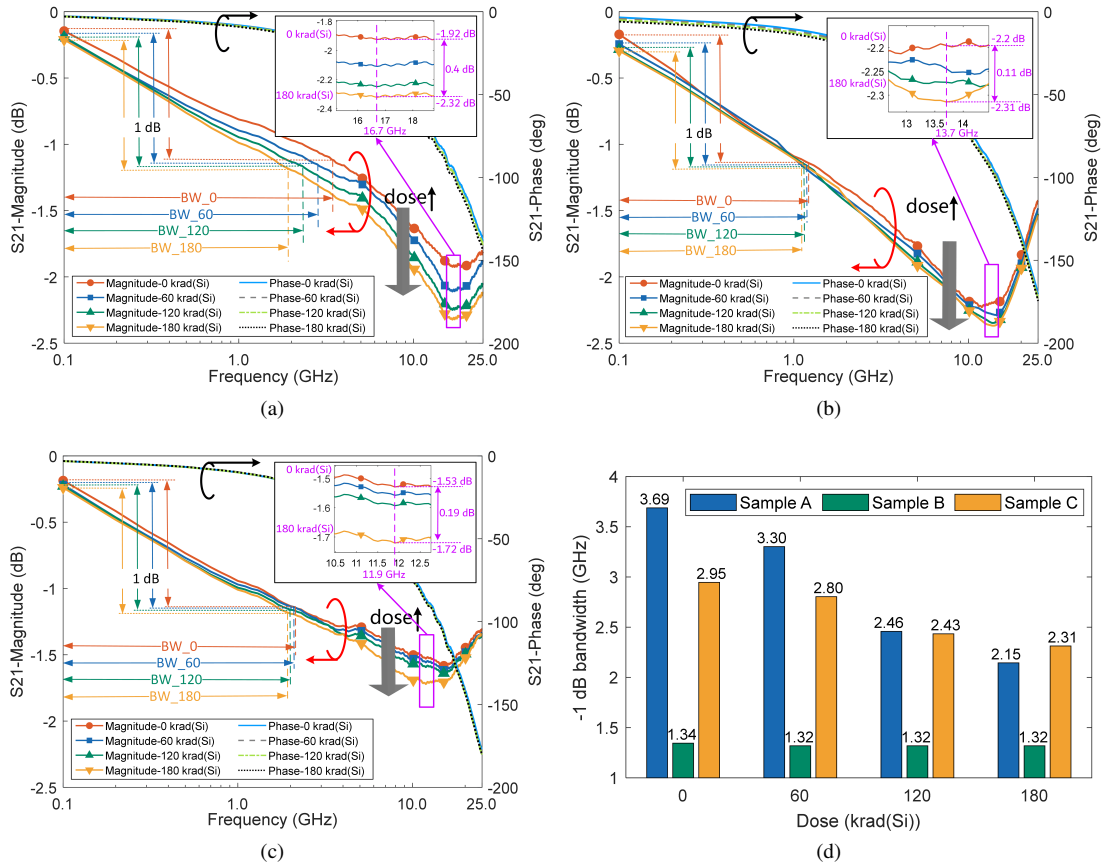


Fig. 5. S_{21} measurement results with dose variation for (a) sample A, (b) sample B, (c) sample C and (d) TID-dependent −1 dB bandwidth of TSV samples.

A pair of 150 μm-pitch GSG probes was mounted on a probe station and connected to a vector network analyzer (VNA) via high-frequency cables. The probes and the TSV chips to be tested are shown in Fig. 4(b). The VNA operated across a frequency range of 0.1–25 GHz with a step size of 0.1 GHz and a 50 Ω port impedance. To mitigate errors from factors such as probe pressure and positioning, S-parameters were averaged across three identical samples for each measurement.

III. EXPERIMENTAL RESULTS AND ANALYSIS

This section analyzes the SI performance of three types of TSV samples under γ-ray irradiation, highlighting the influence of design parameters and irradiation effects on key metrics such as $|S_{21}|$, −1 dB BW, group delay and propagation delay.

A. Variation of S-parameters and −1 dB bandwidth under γ-ray irradiation

The insertion loss and −1 dB BW of the TSV samples were analyzed, as shown in Fig. 5. The −1 dB BW is defined as the frequency range up to the highest frequency where the insertion loss increases by 1 dB relative to the DC level.

Figs. 5(a) – 5(c) illustrate the S_{21} for samples A, B, and C at irradiation doses of 60, 120, and 180 krad(Si). Across the 0.1–25 GHz range, $|S_{21}|$ initially decreases, reaching a minimum, before increasing at higher frequencies. At 180 krad(Si), the minimum $|S_{21}|$ occurs at 16.7 GHz for sample A (−2.32 dB), 13.7 GHz for sample B (−2.31 dB), and 11.9 GHz for sample C (−1.72 dB). In all cases, $|S_{21}|$ decreases with increasing irradiation dose, indicating greater signal attenuation due to TID effects. The phase of S_{21} ($\angle S_{21}$) shown exhibits minimal variation with irradiation dose and displays a nonlinear relationship with frequency.

The relative decrease in $|S_{21}|$ varies among the samples from 0 to 180 krad(Si). Sample A exhibits the largest reduction (0.4 dB at 16.7 GHz), primarily attributed to its silicon FMSS and narrow spacing ($p_{\mathrm{STSV}} = 500\,\mu$m), which increases parasitic capacitance (C_{Si}) and conductance (G_{Si}) [54]. Radiation further elevates the relative permittivity ($\varepsilon_{\mathrm{Si}}$) and conductivity ($\sigma_{\mathrm{Si}}$) of the silicon substrate. Sample B shows the smallest degradation (0.11 dB at 13.7 GHz), owing to its wider spacing $p_{\mathrm{STSV}} = 1000\,\mu$m and its silicon and EMC FMSS, which reduces electric field coupling and mitigates dielectric degradation. Sample C, which shares the same $p_{\mathrm{STSV}} = 500\,\mu$m as sample A but uses silicon and EMC

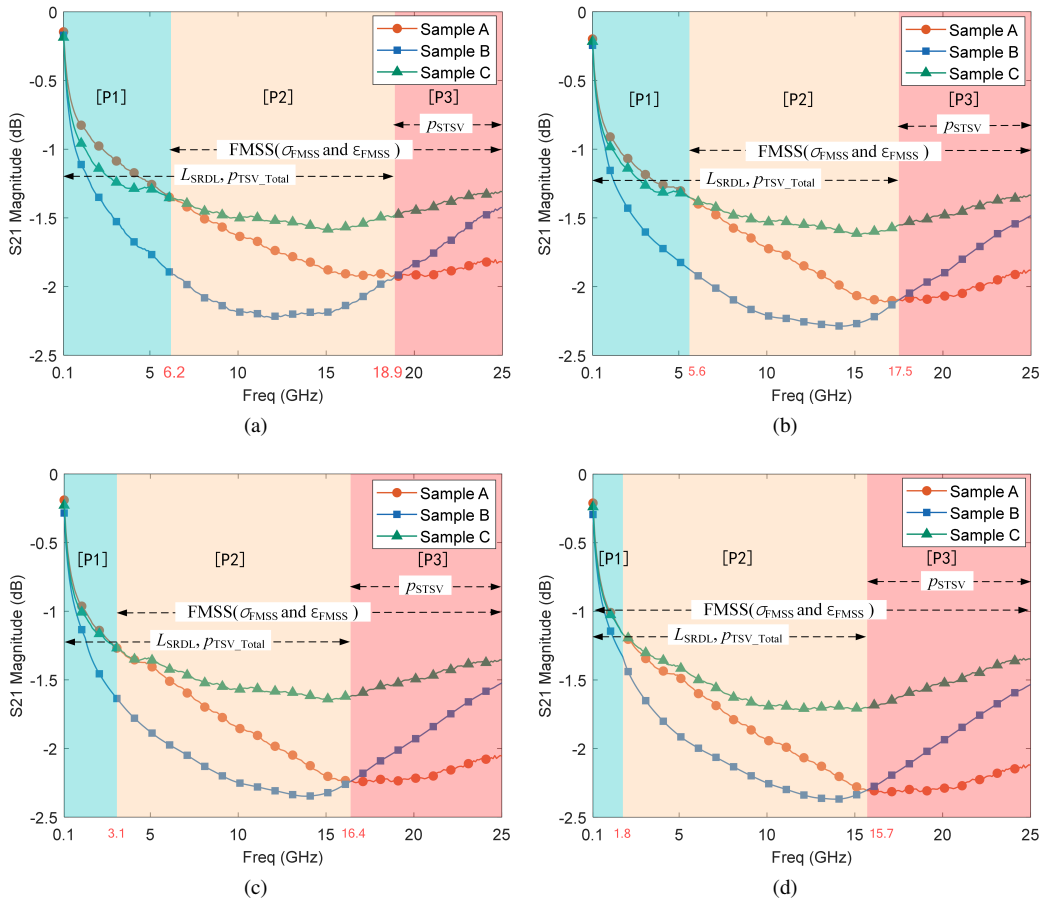


Fig. 6. Frequency response related to design factors of TSV samples at (a) 0 krad(Si); (b) 60 krad(Si); (c) 120 krad(Si) and (d) 180 krad(Si).

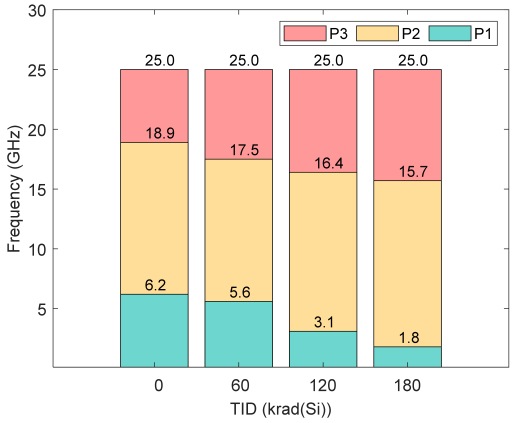


Fig. 7. TID-Induced frequency response compression in TSV samples: With increasing dose, P1, P2 and P3 boundaries shift to lower frequencies.

FMSS, experiences a moderate S_{21} decrease (0.19 dB at 11.9 GHz), benefiting from improved isolation.

The voltage and power transfer efficiencies were computed using Eqs. (2) and (3), with S_{21} converted from dB to linear values via Eq. (1) [55]. At 180 krad(Si) and the frequency of minimum $|S_{21}|$, the voltage transfer efficiency decreases by 4.50% (A), 1.26% (B), and 2.16% (C), while power transfer efficiency declines by 8.80% (A), 2.50% (B), and 4.28% (C) relative to pre-irradiation values.

$$|S_{21}|_{\text{linear}} = 10^{\frac{|S_{21}|_{\text{dB}}}{20}} \tag{1}$$

$$\eta_{\text{Voltage}} = \frac{|S_{21}^{0}|_{\text{linear}} - |S_{21}^{180}|_{\text{linear}}}{|S_{21}^{0}|_{\text{linear}}} \tag{2}$$

$$\eta_{\text{Power}} = \frac{|S_{21}^{0}|_{\text{linear}}^{2} - |S_{21}^{180}|_{\text{linear}}^{2}}{|S_{21}^{0}|_{\text{linear}}^{2}} \tag{3}$$

At 15 GHz, S_{21} of Sample A decreases from −1.87 dB (0 krad) to −2.27 dB (180 krad), while Sample C decreases from −1.58 dB to −1.70 dB. Although Sample A has a shorter $l_{\text{SRDL}} = 1700\mu$m which typically reduces resistive loss [56, 57], its silicon FMSS and smaller p_{STSV} increase crosstalk, leading to a more significant degradation in S_{21} compared to sample C.

As shown in Fig. 5(d), Sample A initially has the widest −1 dB BW, while Sample B has the narrowest. However,

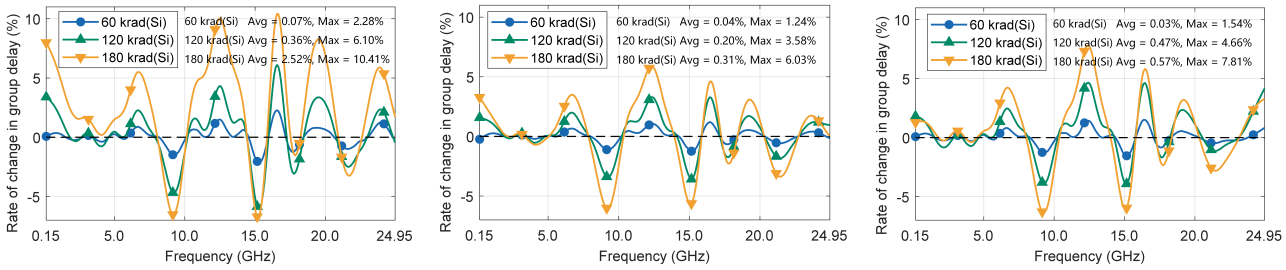


Fig. 8. Variation of TID-induced group delay in TSV samples relative to pre-irradiation: (a) Sample A, (b) Sample B, (c) Sample C. Avg represents the average rate of change and Max represents the maximum rate of change.

at 180 krad(Si), BWs decrease by 41.73% (A), 1.49% (B), and 21.69% (C), suggesting worsened inter-symbol interference (ISI) suppression. After 120 krad(Si), sample C's BW exceeds that of sample A, indicating better ISI resilience at higher irradiation doses due to its FMSS composition.

B. Variation of frequency response of design parameters-related under γ-ray irradiation

To investigate the influence of design parameters on the frequency response of TSVs under γ-ray irradiation, this study examines the effects of p_{STSV}, $p_{\mathrm{TSV\_Total}}$, l_{SRDL}, and the properties of the FMSS (σ_{FMSS} and $\varepsilon_{\mathrm{FMSS}}$) across varying TID levels. As shown in Fig. 6, the frequency range (0.1–25 GHz) is divided into three bands—low (P1), mid (P2), and high (P3)—based on the $|S_{21}|$ intersection points. At 0 krad(Si), these bands are P1 (0–6.2 GHz), P2 (6.2–18.9 GHz), and P3 (18.9–25.0 GHz). With increasing TID, the bands compress significantly: at 180 krad(Si), they shift to P1 (0–1.8 GHz), P2 (1.8–15.7 GHz), and P3 (15.7–25.0 GHz), as shown in Fig. 7, reflecting a TID-induced redistribution of the frequency response.

As presented in Table 1, samples A and C share identical p_{STSV} and $p_{\mathrm{TSV\_Total}}$, but differ in l_{SRDL}. Sample A, with a shorter l_{SRDL}, is expected to exhibit lower insertion losses, potentially improving $|S_{21}|$ [54]. However, in sample A, the two STSVs are integrated on the same silicon substrate, i.e. the FMSS is silicon, which increases the crosstalk between the STSVs, resulting in lower $|S_{21}|$ in P2 and P3 than in sample C, as shown in Fig. 6. Therefore, the properties of the FMSS are the main factor affecting the $|S_{21}|$ in these bands.

Comparing samples A and B, sample A features a larger $p_{\mathrm{TSV\_Total}}$ but a smaller p_{STSV}. While the larger $p_{\mathrm{TSV\_Total}}$ theoretically reduces substrate leakage, the smaller p_{STSV} and silicon as an FMSS in Sample A amplifies the crosstalk, resulting in a lower $|S_{21}|$ in P3. Here p_{STSV} is the main factor as the wider pitch of STSV in Sample B reduces the coupling effect. The silicon and EMC as FMSS of sample B further reduces σ_{FMSS} and increases the stability of $|S_{21}|$.

In P1 and P2, Sample A benefits from its shorter l_{SRDL} and larger $p_{\mathrm{TSV\_Total}}$, achieving higher $|S_{21}|$ compared to sample B . For Samples B and C, despite Sample B's larger p_{STSV} reducing crosstalk, its smaller $p_{\mathrm{TSV\_Total}}$ ($2(1+2\sqrt{2})p_{\mathrm{TSV}}$) increases substrate leakage, leading to lower $|S_{21}|$ in P1 and P2. Thus, l_{SRDL} and $p_{\mathrm{TSV\_Total}}$ collectively dominate $|S_{21}|$ variations in these bands.

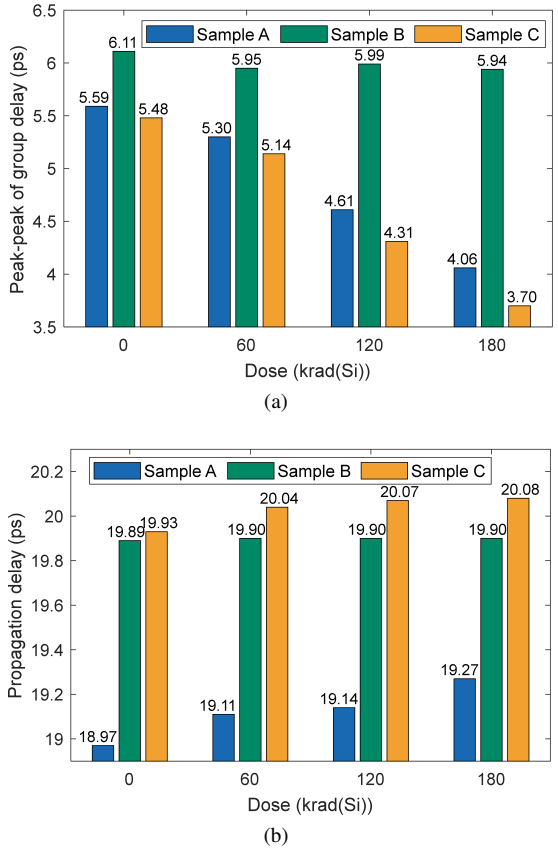


Fig. 9. TID dependent changes in (a) peak-to-peak of group delay and (b) propagation delay.

In summary, the variation in $|S_{21}|$ across different frequency bands is primarily determined by design parameters. As the irradiation dose increases, the compression effect on the $|S_{21}|$ frequency response causes the design factors dominating $|S_{21}|$ in each band to take effect at lower frequencies earlier than expected.

C. Variation of group delay and propagation delay under γ-ray irradiation

The impact of TID radiation on TSV signal transmission timing can be analyzed through the evolution of group delay and propagation delay. Group delay (τ_{group}) is defined as the negative derivative of the phase response with respect to frequency, representing the rate of phase change of a signal near a given angular frequency ω, as expressed in Eq. (4) [58].

$$\tau_{\text{group}} = -\frac{\mathrm{d}\phi(\omega)}{\mathrm{d}\omega} \tag{4}$$

The peak to peak of group delay (τ_{ppgd}) is the difference between the maximum and minimum group delay across the entire frequency band, representing the fluctuation amplitude of group delay, as given in Eq. (5).

$$\tau_{\text{ppgd}} = \max(\tau_{\text{group}}) - \min(\tau_{\text{group}}) \tag{5}$$

Propagation delay (τ_{prop}) represents the total transmission time from input to output and can be derived using the inverse Fourier transform of the S-parameters. It is specifically defined as the time shift of the peak in the impulse response, as given in Eq. (6) and (7) [58].

$$h(t, D) = \text{IFFT}\left\{|S_{21}(f, D)| \cdot e^{j\phi(f,D)}\right\} \tag{6}$$

$$\tau_{\text{prop}}^{D} = \arg\max_{t} |h(t, D)| \tag{7}$$

As shown in Figs. 8(a) – 8(c), the group delay variation rate of all three TSV samples increases significantly with radiation dose, indicating that TID-induced cumulative damage alters the phase response characteristics of TSVs. At 180 krad(Si), sample A exhibits the highest average group delay variation rate (2.52%), while sample B shows the lowest (0.31%). This difference is attributed to sample A's single silicon material filling and smaller p_{STSV}, which increase electric field coupling and radiation sensitivity. Conversely, sample B's larger p_{STSV} and EMC composite filling enhance stability by reducing coupling and suppressing dielectric constant fluctuations. Sample C, despite using the same composite material as sample B, shows a average variation rate of 0.57% due to its denser STSV layout, highlighting the detrimental effect of close TSV spacing in high-radiation environments.

The τ_{ppgd} of all samples decreases with increasing irradiation dose, as shown in Fig. 9(a). This suggests that TID radiation reduces delay variance, potentially weakening phase non-linearity. At 180 krad(Si), the maximum reduction in τ_{ppgd} is 32.48% (A) compared to pre-irradiation. This finding highlights a trade-off between phase linearity and transmission loss in irradiation tolerant designs.

As shown in Fig. 9(b), the propagation delay of sample A increases by 1.58% at 180 krad(Si), primarily due to its smaller p_{STSV} and single silicon filling, which enhance electric field coupling. Sample B exhibits the most stable propagation delay, with a fluctuation range of less than 0.05%, attributed to its larger p_{STSV} and EMC composite filling. Sample C shows an intermediate increase of 0.75%, indicating that composite filling partially mitigates the radiation sensitivity of a small p_{STSV} layout.

The stability of propagation delay in TSV chips is influenced by both TSV layout parameters (p_{STSV}) and material properties (FMSS). Optimizing p_{STSV} and employing suitable composite filling materials (such as silicon and EMC) significantly enhances irradiation resistance. For irradiation tolerant designs, a balanced approach is required to maintain signal integrity while minimizing time domain jitter and phase nonlinearity to ensure high reliability TSV interconnects.

IV. ELECTRICAL MODELING OF THE TSV CHANNEL

The TSV channel consists of four primary materials: copper for the TSVs, bumps, and RDLs; silicon for the substrates; silicon dioxide as a thin insulating layer surrounding the TSVs; and an EMC as the isolation material. TID irradiation alters the material properties, including the conductivity of copper, the conductivity and dielectric constant of the silicon substrate, and the dielectric constant of the oxide layer. To evaluate the impact of TID irradiation on TSV channel performance, a TID-dependent TSV model is required. This model must also account for additional factors, such as the significantly greater length of the RDLs compared to the height of the TSVs.

A. Equivalent circuit Modeling

Fig. 10(a) presents the TSV channel model for the three test sample types. It consists of three main components: the top RDL used for probing, the TSV structure, and the bottom RDL serving as an interconnection point. Fig. 10(b) provides a detailed representation of the RDL models at the top and bottom of the TSV. Due to the symmetrical arrangement of the RDLs, only one top-layer RDL model is shown in Fig. 10(b). Table 3 summarizes the electrical parameters of the TSV channel model.

Both the RDLs and TSVs, made of copper, are represented as a series of resistances and inductances. This representation accounts for the conductive losses and the magnetic energy storage in these structures. The TSVs are coated with a thin layer of silicon dioxide, which is modeled as a capacitor. This capacitor represents the charge storage capability of the insulating layer between the conductive TSV and the silicon substrate. The silicon substrate is modeled as a parallel network of resistors and capacitors. The substrate capacitance C_{Sub} and resistance R_{Sub} between an STSV and a GTSV are represented by Eqs. (8) and (9), respectively [59]. These equations are derived based on the quasi-static approximation of the electric field distribution between cylindrical conductors

Table 3. Description of parameter symbols.

Symbol	Description	Symbol	Description
$R_{\mathrm{RDL\_Top}}$	Resistance of top RDL	$C_{\mathrm{RDL\_Top}}$	Capacitance of top RDL
$R_{\mathrm{RDL\_Bot}}$	Resistance of bottom RDL	$C_{\mathrm{RDL\_Bot}}$	Capacitance of bottom RDL
$R_{\mathrm{Si\_RDL}}$	Resistance of top RDL to silicon substrate	C_{Fill}	Capacitance of top RDL to EMC
$L_{\mathrm{RDL\_Top}}$	Inductance of top RDL	$L_{\mathrm{RDL\_Bot}}$	Inductance of bottom RDL
R_{TSV}	Resistance of TSV	L_{TSV}	Inductance of Top
C_{oxs}	Capacitance of oxide layer of STSV	C_{oxg}	Capacitance of oxide layer of GTSV
R_{Si}	Resistance of silicon substrate	C_{Si}	Capacitance of silicon substrate
$R_{\mathrm{Crosstalk}}$	Resistance of crosstalk of STSV-STSV	$C_{\mathrm{Crosstalk}}$	Capacitance of crosstalk of STSV-STSV
C_{Bump}	Capacitance of bump		

in a dielectric medium [54]. Eq. (10) [60] expresses the inherent relationship between the capacitance and conductance of the silicon substrate, linking its permittivity and conductivity.

$$C_{\mathrm{Sub}} = \frac{\pi\varepsilon_0\varepsilon_{\mathrm{Si}}}{cosh^{-1}(p_{\mathrm{TSV}}/d_{\mathrm{TSV}})} \times h_{\mathrm{TSV}} \tag{8}$$

$$R_{\mathrm{Sub}} = \frac{cosh^{-1}(p_{\mathrm{TSV}}/d_{\mathrm{TSV}})}{\pi\sigma_{\mathrm{Si}}h_{\mathrm{TSV}}} \tag{9}$$

where ε_0 is the permittivity of vacuum, $\varepsilon_{\mathrm{Si}}$ is the relative permittivity of silicon, σ_{Si} is the conductivity of silicon, p_{TSV} is the center-to-center pitch between the STSV and the nearest GTSVs (250 μm), and d_{TSV} is the TSV diameter.

$$\frac{C_{\mathrm{Sub}}}{G_{\mathrm{Sub}}} = \frac{\varepsilon_{\mathrm{Si}}}{\sigma_{\mathrm{Si}}} \tag{10}$$

When mapping this model to the GSG-type equivalent circuit shown in Fig. 10(a), adjustments are made to account for the specific distribution of GTSVs around the STSV in the different sample designs. The equivalent resistances and capacitances for samples A, B, and C are calculated using Eqs. (8) and (9) and the $p_{\mathrm{STSV\_Total}}$ values defined in Fig. 2. The scaling factors in these equations are derived from the specific geometrical arrangements of the GTSVs around the central STSV for each sample type. For example, the resistances for samples A and C are given by:

$$R_{\mathrm{Si}}^{\mathrm{A}} = R_{\mathrm{Si}}^{\mathrm{C}} = \frac{R_{\mathrm{sub}}}{1+\sqrt{2}+\sqrt{5}} \tag{11}$$

with corresponding capacitances:

$$C_{\mathrm{Si}}^{\mathrm{A}} = C_{\mathrm{Si}}^{\mathrm{C}} = (1+\sqrt{2}+\sqrt{5})C_{\mathrm{sub}} \tag{12}$$

For sample B:

$$R_{\mathrm{Si}}^{\mathrm{B}} = \frac{R_{\mathrm{sub}}}{1+2\sqrt{2}} \tag{13}$$

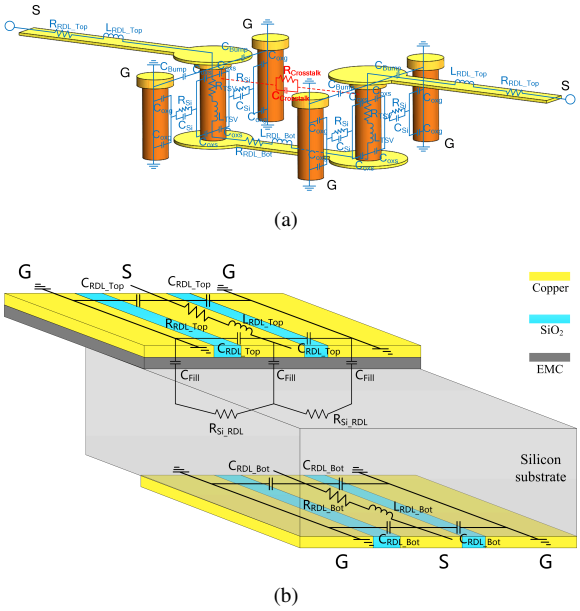


Fig. 10. GSG-type equivalent circuit model of (a) TSV channel and (b) RDL layer for conducting an optimization design in ADS to quantitatively investigate the impact of TID on the electrical parameters of the TSV channel.

And the C_{Si} is calculated as

$$C_{\mathrm{Si}}^{\mathrm{B}} = (1+2\sqrt{2})C_{\mathrm{sub}} \tag{14}$$

The connections between GTSVs and STSVs are represented by an RC network, and crosstalk between STSVs is accounted for using an additional RC model, highlighted by the red dashed lines in Fig. 10(a). The crosstalk capacitance ($C_{\mathrm{Crosstalk}}$) and resistance ($R_{\mathrm{Crosstalk}}$) between adjacent STSVs are described by Eqs. (15) and (16) [50, 51, 59], based on the quasi-static approximation of the electric field distribution between two parallel cylindrical conductors. Here, p_{STSV} represents the center-to-center pitch between the two STSVs, and $\varepsilon_{\mathrm{FMSS}}$ and σ_{FMSS} represent the relative permittivity and conductivity of the filling material (FMSS) between them, respectively. As illustrated in Fig. 1, for sample A, both STSVs are located within the same silicon substrate ($\varepsilon_{\mathrm{FMSS}}$ = $\varepsilon_{\mathrm{Si}}$, σ_{FMSS} = σ_{Si}). Conversely, in samples B and C, the two

STSVs are situated in separate silicon substrates, separated by an EMC layer. For these two samples, $\varepsilon_{\mathrm{FMSS}}$ is lower than $\varepsilon_{\mathrm{Si}}$, and σ_{FMSS} is significantly lower than σ_{Si}.

$$C_{\mathrm{Crosstalk}} = \frac{\pi\varepsilon_0\varepsilon_{\mathrm{FMSS}}}{cosh^{-1}(p_{\mathrm{STSV}}/d_{\mathrm{TSV}})} \times h_{\mathrm{TSV}} \tag{15}$$

$$R_{\mathrm{Crosstalk}} = \frac{cosh^{-1}(p_{\mathrm{STSV}}/d_{\mathrm{TSV}})}{\pi\sigma_{\mathrm{FMSS}}h_{\mathrm{TSV}}} \tag{16}$$

Fig. 10(b) also provides a more detailed model of the RDL structure. The SRDL connects the horizontally aligned STSVs, while the GRDL connects the horizontally aligned GTSVs. These components are electrically isolated by an insulating layer, which is represented as a capacitor in the model. Additionally, the top RDL is separated from the silicon substrate by an EMC layer, which is also modeled as a capacitor. To account for the penetration of the electric field into the dielectric layers and the silicon substrate beneath the RDL, the model incorporates the effective conductivity of the silicon substrate.

The resistance of a TSV, R_{TSV}, comprises both DC and AC components, as described in Eqs. (17) – (20) [54, 59–61]. At high frequencies, the skin effect causes current to concentrate near the conductor's surface. Furthermore, the proximity effect, influenced by adjacent conductors, alters current distribution, leading to a non-uniform peripheral profile. As TSVs are placed closer together, the proximity factor, k_{p} increases. For TSVs, k_{p} is determined by the ratio of the TSV pitch p_{TSV} to the TSV diameter d_{TSV} [54].

$$R_{\mathrm{TSV}} = \sqrt{R^2_{\mathrm{dc\_TSV}} + R^2_{\mathrm{ac\_TSV}}} \tag{17}$$

where

$$R_{\mathrm{dc\_TSV}} = \rho_{\mathrm{TSV}} \times \frac{h_{\mathrm{TSV}}}{\pi \times r^2_{\mathrm{TSV}}} \tag{18}$$

$$R_{\mathrm{ac\_TSV}} = k_{\mathrm{p}} \left(\rho_{TSV} \times \frac{h_{TSV}}{2\pi r_{\mathrm{TSV}}\delta_{\mathrm{skindepth}} - \pi\delta^2_{\mathrm{skindepth}}} \right) \tag{19}$$

$$\delta_{\mathrm{skindepth}} = \frac{1}{\sqrt{\pi f \mu_{\mathrm{TSV}}\sigma_{\mathrm{TSV}}}} \tag{20}$$

where, $\delta_{\mathrm{skindepth}}$ is the skin depth. k_{p} is the proximity factor.

Similarly, the bump resistance is calculated using both DC and AC components, consistent with the TSV resistance model. Moreover, the capacitance between a signal bump and a ground bump, $C_{\mathrm{Bump\_GS}}$, is calculated using a modified parallel plate model adjusted for cylindrical geometry, as expressed in Eq. (21) [54].

$$C_{\mathrm{Bump\_GS}} = \frac{\pi \times \varepsilon_0\varepsilon_{\mathrm{EMC}}}{\cosh^{-1}\left(\frac{p_{\mathrm{TSV}}}{d_{\mathrm{Bump}}}\right)} \times h_{\mathrm{Bump}} \tag{21}$$

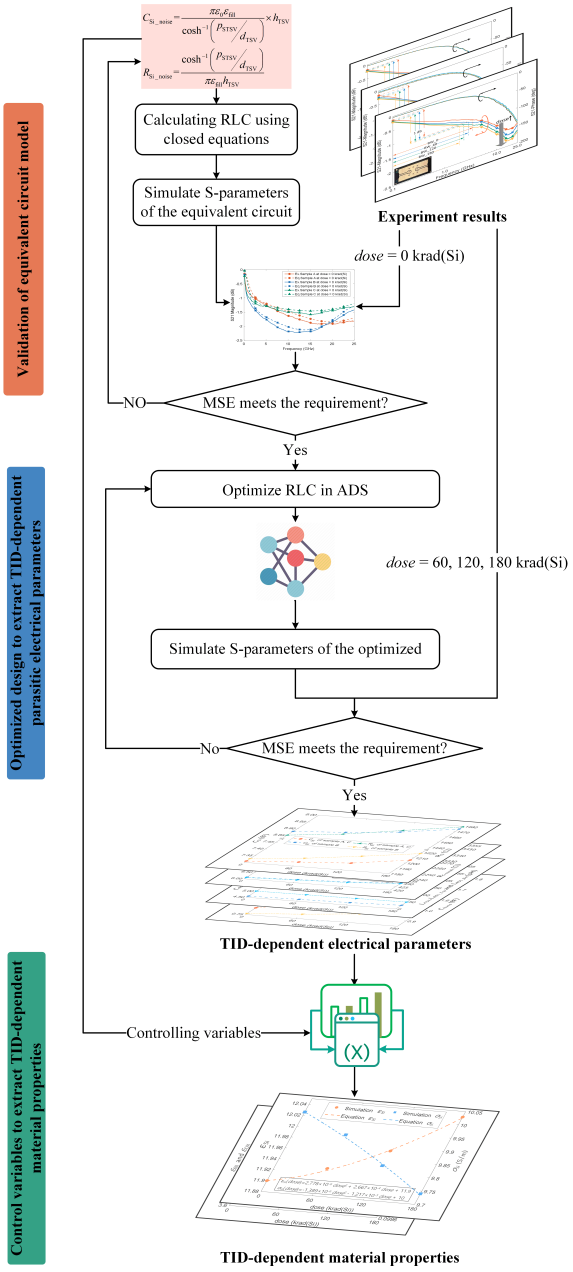


Fig. 11. Verification of the equivalent circuit model at 0 krad(Si) for the process of extracting TID dependent electrical parameters and material properties.

where, $\varepsilon_{\mathrm{EMC}}$ is the relative permittivity of the EMC.

The method for mapping Eq. (21) to C_{Bump} in the GSG model shown in Fig. 10(a), based on the distribution of GTSVs around an STSV in different sample designs, is analogous to the approach used for mapping C_{sub} to C_{Si}.

As shown in Fig. 13(d), C_{Bump} increases with irradiation dose for all three TSV sample types. This trend is attributed to the radiation-induced rise in $\varepsilon_{\mathrm{FMSS}}$. At high frequencies, the capacitive impedance $Z_{C_{\mathrm{Bump}}} = 1/j\omega C_{\mathrm{Bump}}$ decreases as C_{Bump} increases, leading to greater signal leakage through C_{Bump} to ground. This leakage reduces the output signal en-

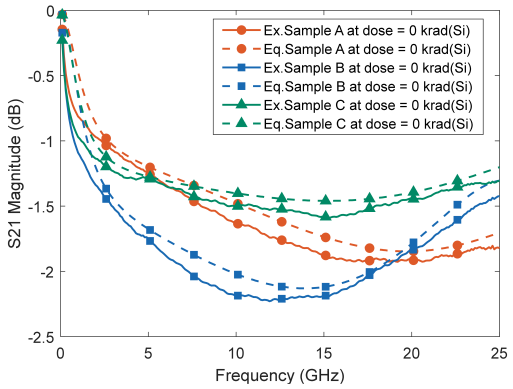


Fig. 12. Comparison of $|S_{21}|$ obtained by experiment and the equivalent circuit model. The validated TSV channel models at 0 krad(Si) are employed for extracting the electrical parameters of the equivalent circuit at doses of 60, 120, and 180 krad(Si), as well as determining the variation of material properties with dose based on the extracted electrical parameters coupled with closed-form equations.

ergy, thereby increasing insertion loss.

In GSG-type TSVs, the capacitance (C_{oxg}) of the oxide layer in the GTSV was determined through full-wave simulation and is approximately 1.5 times C_{oxs}. The value of C_{oxs} was calculated using Eq. (22) [54, 59].

$$C_{\mathrm{oxs}} = \frac{1}{2} \times \frac{\pi \varepsilon_0 \varepsilon_{\mathrm{ox}} h_{\mathrm{TSV}}}{ln((r_{\mathrm{TSV}} + t_{\mathrm{ox}})/r_{\mathrm{TSV}})} \tag{22}$$

where, $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the oxide layer and t_{ox} is the thickness of the oxide layer.

The capacitance models for the RDL interconnects ($C_{\mathrm{RDL\_Top}}$, $C_{\mathrm{RDL\_Bot}}$, and C_{Fill}) are more complex. To compute these capacitances, the conformal mapping method is employed, which utilizes the complete elliptical integral of the first kind, as detailed in [54, 59]. Other electrical parameters of the TSV channel were calculated based on the methodology described in [54].

B. Extraction of TID dependent parasitic electrical parameters

At pre-irradiation (dose = 0 krad(Si)), the electrical parameters of the equivalent circuit model were calculated using closed-form equations based on device dimensions and material properties. However, as the irradiation dose increased, these parameters varied, necessitating an iterative optimization process. To assess TID effects comprehensively, the equivalent circuit model, depicted in Fig. 10, was developed and optimized using Advanced Design System (ADS). Fig. 11 demonstrates the pre-irradiation validation of the model, followed by the extraction of TID-dependent parasitic parameters and material properties. The optimization minimized the mean square error (MSE) between simulated and experimentally measured S-parameters.

Fig. 12 compares the $|S_{21}|$ obtained from experimental measurements and the equivalent circuit model. The MSE values for samples A, B, and C were 0.0177, 0.0222, and 0.0143, respectively. These low MSE values demonstrate a strong correlation between the model and experimental data, validating the accuracy of the proposed TSV channel model.

The impedance of the TSV along the leakage path to the silicon substrate is modeled as a parallel combination of R_{Si} and C_{Si}, as expressed in Eq. (23), with its magnitude given by Eq. (24) [55].

$$Z = \left(\frac{1}{R} + j\omega C \right)^{-1} \tag{23}$$

$$|Z| = \frac{R}{\sqrt{1 + (\omega RC)^2}} \tag{24}$$

At high frequencies, the denominator of $|Z|$ is dominated by the $(\omega RC)^2$ term. Since the S-parameter measurements in this study were conducted in the GHz range, Eq. (24) can be approximated by Eq. (25) [55]. This approximation indicates that, under high-frequency conditions, $|Z|$ is primarily determined by the capacitance C and is inversely proportional to it.

$$|Z| \approx \frac{1}{\omega C} \tag{25}$$

Fig. 13 presents the extracted electrical parameters under varying radiation doses. Notably, Fig. 13(a) shows increases in both C_{Si} and R_{Si} of the three types of TSV samples increase with increasing radiation dose. This trend results in a decrease in the impedance $|Z|$, which consequently leads to an increase in insertion loss. This phenomenon is a significant contributing factor to the experimental results observed in Fig. 5.

Similarly, Fig. 13(b) shows that $C_{\mathrm{Crosstalk}}$ and $R_{\mathrm{Crosstalk}}$ also increased with dose, further contributing to insertion loss via reduced impedance along the leakage path to the FMSS. Notably, the FMSS materials in samples B and C (EMC and silicon) exhibit lower conductivity compared to the silicon used in sample A, resulting in significantly higher $R_{\mathrm{Crosstalk}}$ for samples B and C.

The parameters $C_{\mathrm{RDL\_Top}}$, $C_{\mathrm{RDL\_Bot}}$, C_{Fill}, L_{TSV}, $L_{\mathrm{RDL\_Top}}$, and $L_{\mathrm{RDL\_Bot}}$ were identical across all three sample types and consistent with the methodology outlined in [54, 59]. As the dose increased, all parameters exhibited growth, with the inductances of the top and bottom RDLs showing more pronounced changes than the other parameters, as shown in Fig. 13(c). Additionally, Fig. 13(d) shows that both C_{oxs} and C_{Bump} increased with dose. Since C_{Bump} depends on the arrangement of GTSVs surrounding the STSV (Fig. 1), samples A and C, which share the same GTSV configuration, showed identical C_{Bump} values.

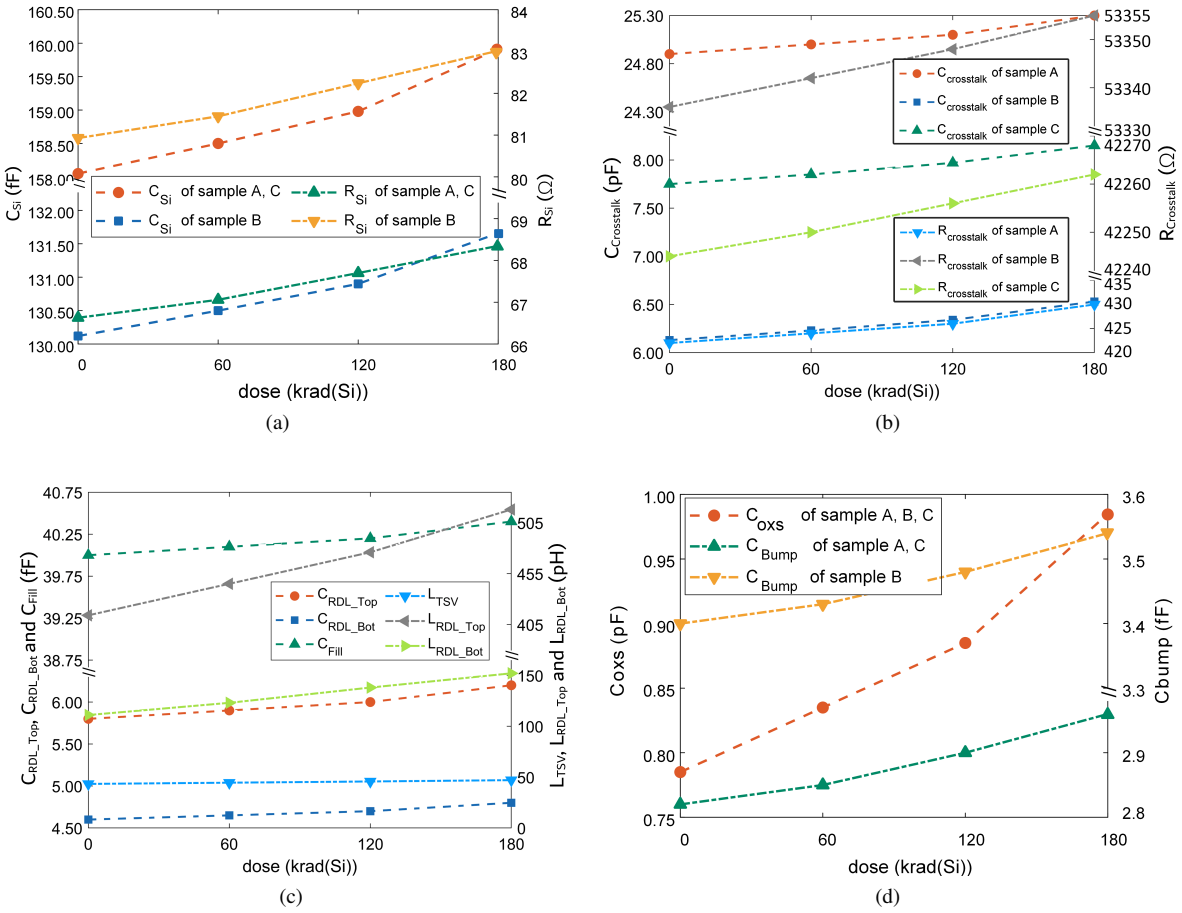


Fig. 13. Impact of TID on electrical parameters for TSV channel: (a) C_{Si} and R_{Si}, (b) $C_{\mathrm{Crosstalk}}$ and $R_{\mathrm{Crosstalk}}$, (c) $C_{\mathrm{RDL\_Top}}$, $C_{\mathrm{RDL\_Bot}}$, C_{Fill}, L_{TSV}, $L_{\mathrm{RDL\_Top}}$ and $L_{\mathrm{RDL\_Bot}}$, (d) C_{oxs}, and C_{Bump}. The electrical parameters at 0 krad(Si) are calculated by closed-form equations and those at 60, 120, 180 krad(Si) are obtained by optimization design in ADS.

C. Analysis of changes in properties of TSV materials under γ-ray irradiation

The model validated at 0 krad(Si) in Sect. IV A is employed to extract the parasitic electrical parameters of the TSV channel under TID radiation, as shown in Fig. 11. Additionally, it facilitates the estimation of TID-induced effects on the material properties of TSV channels through closed-form equations.

The electrical parameters of the TSV channel include geometric parameters (such as TSV radius, height, and pitch) and material properties (such as dielectric constant and conductivity). In the absence of TID-induced mechanical stress, the geometric parameters remain constant, while only material properties are affected. Consequently, the variations in electrical parameters shown in Fig. 13 are attributed to TID-induced changes in material properties. Based on this observation, the TID-dependent material properties presented in Fig. 14 were derived following the process shown in Fig. 11, establishing a quadratic relationship between material properties and irradiation dose. This enhancement transforms the calculation of electrical parameters in the TSV model (Fig. 10) from fixed equations to dose-dependent functions, enabling the prediction of signal loss in the TSV channel at varying irradiation doses.

V. FUTURE WORK

The proposed TSV electrical model is developed using a methodology that integrates design parameters and TID effects. This model serves two primary purposes: predicting the frequency response of TSVs under TID irradiation and rapidly generating datasets for training machine learning models, which will be a focus of our future work. At this stage, the lack of TID-related data—such as DC, AC, C-V characteristics, impedance measurements, and time-domain eye diagrams—limits the model. Furthermore, the model does not incorporate electrical stress or process parameters, such as doping, which are crucial for developing a more comprehensive and accurate TSV model. Nevertheless, the contribution of this paper is still novel compared to the existing research literature, both in terms of the measured parameters, the analysed parameters and the modeling approach, as shown

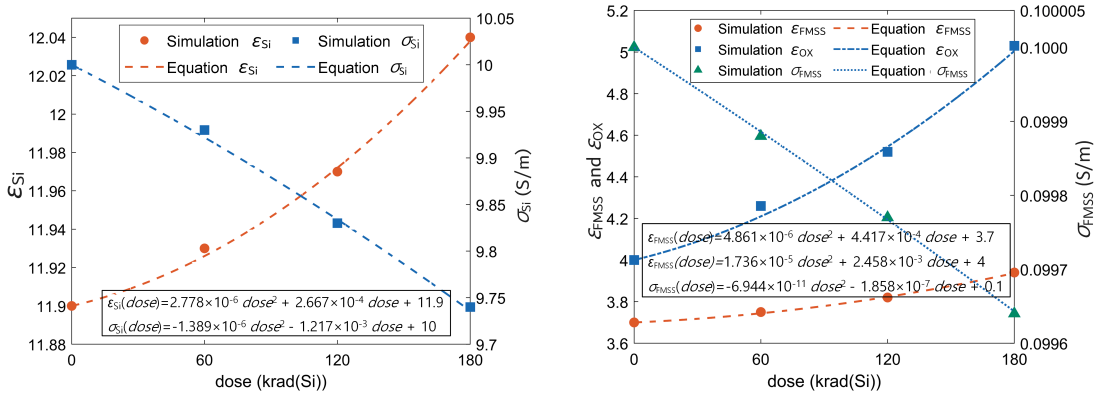


Fig. 14. TID-dependent equations for TSV material properties of (a) $\varepsilon_{\mathrm{Si}}$ and σ_{Si} (b) $\varepsilon_{\mathrm{FMSS}}$, $\varepsilon_{\mathrm{OX}}$ and σ_{FMSS}. Ignoring the variation of mechanical stresses, the TSV channel dimensions are fixed. The variation of the electrical parameters in Fig. 13 is caused by the changes in material properties (scattered dots) due to the TID radiation. The correlation equation between material properties (dashed lines, dot - dash line and double-dash line) and dose was obtained by polynomial fitting.

Table 4. Comparison of this paper with other studies.

Study	Irradiation doses (krad(Si))	Measured parameters	Chip types	Analyzed characteristics	Modeling approach	Crosstalk of STSV	Material properties
Refs. [38, 39]	50	I_{Leak} and C_{TSV}	1	$C-V$ and $I-V$	–	No	No
Ref. [42]	180, 240, 300, 420, 540	$\lvert S_{21}\rvert$ and $\lvert S_{11}\rvert$	1	$\lvert S_{21}\rvert$-freq and $\lvert S_{11}\rvert$-freq	Equivalent circuit model in ADS (coarse grained)	No	No
Ref. [43]	30, 90, 150	$\lvert S_{21}\rvert$	3	$C-V$ and $\lvert S_{21}\rvert$-freq	COMSOL for $C-V$	No	No
Ref. [44]	30, 90, 150	$\lvert S_{21}\rvert$	3	$C-V$ and $\lvert S_{21}\rvert$-freq	1D COMSOL for capacitance, HFSS for S_{21}	No	No
Ours	**0, 60, 120, 180**	$\lvert \boldsymbol{S_{21}}\rvert$ **and** $\angle \boldsymbol{S_{21}}$	**3**	$\lvert \boldsymbol{S_{21}}\rvert$**-freq**, $\angle \boldsymbol{S_{21}}$**-freq**, **−1 dB BW**, $\boldsymbol{\tau_{\mathrm{group}}}$, $\boldsymbol{\tau_{\mathrm{ppgd}}}$ and $\boldsymbol{\tau_{\mathrm{prop}}}$	**TID dependent equivalent circuit model in ADS (fine grained)**	**Yes**	**Yes**

$^{I_{\mathrm{Leak}}}$ Leakage current of TSV.
$^{C_{\mathrm{TSV}}}$ Capacitance of TSV.
$^{|S_{21}|}$ Magnitude of S_{21}.
$^{|S_{11}|}$ Magnitude of S_{11}.
$^{\angle S_{21}}$ Phase of S_{21}.
$^{\mathrm{BW}}$ Bandwidth.

in Table 4. Similar to Refs. [38, 39, 42–45], we do not apply a bias during irradiation. However, we are aware that the irradiation effect can be significantly modulated by the bias. Our future work will address these limitations by obtaining the necessary data and incorporating additional parameters to enhance the model and improve its predictive accuracy.

VI. CONCLUSION

This study comprehensively analyzed the impact of TID irradiation on the TSV channel. By fabricating and testing three types of TSV samples under ^{60}Co γ-ray irradiation, this study demonstrated that TID significantly degraded the electrical performance of TSVs, resulting in greater insertion loss, a narrower -1 dB bandwidth, an increased rate of change of group delay, and extended propagation delay. A TID-induced compression of the frequency response was also observed, shifting the S-parameter variations to lower frequencies. To quantify the TID-induced variations in parasitic electrical parameters, an equivalent circuit model incorporating TSV design parameters and material properties was developed and validated. The model was further optimized in ADS to refine parameter extraction and improve predictive accuracy. The analysis revealed that the variations in parasitic parameters resulted from radiation-induced changes in material properties. Finally, by applying polynomial fitting to establish the relationship between radiation dose and material properties, an electrical model of the TID effect for the TSV channel was established. By formulating the electrical parameters as functions of dose, this model enables the prediction of S-parameters for various TSV designs and radiation conditions, facilitating the evaluation of transmission performance. Despite its predictive accuracy, the model exhibits certain limitations, particularly in high-dose scenarios, where deviations increase and require further refinement. Future work will focus on developing more comprehensive models incorporating multi-physics effects and validating them with additional experimental data. Overall, this study improves the understanding of TID effects on TSVs and provides a theoretical basis for the design of reliable and radiation-tolerant 3D ICs. The results are particularly relevant for aerospace applications and serve as a valuable resource for optimizing TSV designs and predicting performance in radiation environments.

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